PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 0651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	~~Unknown~~ 10/751,135
Filing Date	~~Even Date Herewith~~ 12/30/2003
First Named Inventor	Patel, Bheem
Group Art Unit	~~Unknown~~ 2816
Examiner Name	~~Unknown~~ HAI L. NGUYEN

Sheet 1 of 1

Attorney Docket No: 884.936US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
HLN	US-5,148,381	09/15/1992	Sprague, David L.	364	723	02/07/1991
	US-5,489,864	02/06/1996	Ashuri, Roni	327	161	02/24/1995
	US-5,641,931	06/24/1997	Ogai, Y. , et al.	84	661	03/28/1995
	US-6,073,151	06/06/2000	Baker, J. C., et al.	708	290	06/29/1998
	US-6,121,808	09/01/2000	Gaudet,	327	231	
	US-6,348,826	02/19/2002	Mooney, Stephen R., et al.	327	270	06/28/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
HLN		DONNELLY, K. S., et al., "A 660MB/s Interface Megacell Portable Circuit in -.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 32, (Dec. 1996),1995-2003	
		HAYCOCK, MATTHEW , et al., "A 2.5Gb/s Bidirectional Signaling Technology", Hot Interconnects Symposium V, (Aug. 1997),pp. 1-8	
		LEE, THOMAS H., et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE Journal of Solid-State Circuits, Vol. 29, (Dec. 1994),1491-1496	
		SIDIROPOULOS, STEFANOS , et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, (Nov. 1997),1683-1692	

EXAMINER HAI L. NGUYEN DATE CONSIDERED 02/06/2005

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached